REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** RICK OFFICER	**DEFENSE SUPPLY CENTER, COLUMBUS** **COLUMBUS, OHIO**
Original date of drawing 02-12-12	**CHECKED BY** TOM HESS	**TITLE** MICROCIRCUIT, DIGITAL-LINEAR, 14-BIT, 1, 3, 8 MSPS, ANALOG-TO-DIGITAL CONVERTER, MONOLITHIC SILICON
	APPROVED BY RAYMOND MONNIN	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/03608**
	REV	**PAGE** 1 **OF** 18

AMSC N/A

5962-V008-03

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance analog-to-digital microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/03608	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function	Clock frequency
01	THS1401-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	1 MHz
02	THS1403-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	3 MHz
03	THS1408-EP	14-bit, 8 MSPS DSP compatible analog-to-digital converter with internal reference	8 MHz

1.2.2 Case outline(s). The case outlines shall be as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	48	MS-026	Plastic quad flat pack

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacture:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (AV_{DD} to AGND) ..... 4 V
Supply voltage (DV_{DD} to DGND) ..... 4 V
Reference input voltage range (V_{BG}) ..... -0.3 V to AV_{DD} +0.3 V
Analog input voltage range ..... -0.3 V to AV_{DD} +0.3 V
Digital input voltage range ..... -0.3 V to DV_{DD} +0.3 V
Storage temperature range (T_{STG}) ..... -65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ..... 260°C
Thermal resistance, junction-to-case (θ_{JC}) ..... 0.79°C/W 2/
Thermal resistance, junction-to-ambient (θ_{JA}) ..... 28.8°C/W 2/

1.4 Recommended operating conditions. 3/

Supply voltage range (AV_{DD}, DV_{DD}) ..... 3 V to 3.6 V
High level digital input voltage (V_{IH}) ..... 2 V minimum
Low level digital input voltage (V_{IL}) ..... 0.8 V maximum
Load capacitance (C_L) ..... 15 pF maximum
Clock frequency (f_{CLK}) :
  Device type 01 ..... 0.1 to 1 MHz
  Device type 02 ..... 0.1 to 3 MHz
  Device type 03 ..... 0.1 to 8 MHz
Clock duty cycle ..... 45% to 55%
Operating free-air temperature range (T_A):
  Device types 01 and 02 ..... -40°C to +125°C
  Device type 03 ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at http://www.jedec.org)

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “ recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Informational purposes only, not production tested.
3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Block diagram. The block diagram shall be as shown in figure 3.

3.5.4 Timing diagrams. The timing diagrams shall be as shown in figure 4.

3.5.5 Principles of operation. The principles of operation shall be as shown in figure 5.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supply section							
Analog supply current	I_{DDA}	AV_{DD} = 3.6 V	1/	All		90	mA
Digital supply current	I_{DDD}	DV_{DD} = 3.6 V				10	mA
Power		$AV_{DD} = DV_{DD}$ = 3.6 V				360	mW
Power down current					20 typical		µA
DC characteristics section							
Resolution			1/	All	14 typical		Bits
Differential nonlinearity	DNL					±1	LSB
Integral nonlinearity	INL	Best fit		01		±2.5	LSB
				02		±3	
				03		±7.5	
Offset error	OE	IN+, IN-, PGA = 0 dB		All		0.3	%FSR
Gain error	GE	PGA = 0 dB				1.75	%FSR
AC characteristics section							
Effective number of bits	ENOB		1/	All	11.2		Bits
Total harmonic distortion	THD	f_i = 100 kHz			-81 typical		dB
		f_i = 1 MHz		02,03	-78 typical		
		f_i = 4 MHz		03	-77 typical		
Signal-to-noise ratio	SNR	f_i = 100 kHz		All	72 typical		dB
		f_i = 1 MHz		02,03	70		
		f_i = 4 MHz		03	71 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC characteristics section - continued							
Signal-to-noise ratio + distortion	SINAD	f_i = 100 kHz	1/	All	70 typical		dB
		f_i = 1 MHz		02,03	69		
		f_i = 4 MHz		03	70 typical		
Spurious free dynamic range	SFDR	f_i = 100 kHz		All	80 typical		dB
		f_i = 1 MHz		02,03	71		
		f_i = 4 MHz		03	80 typical		
Analog input bandwidth				All	140 typical		MHz
Reference voltage section							
Bandgap voltage, internal mode	VBG		1/	All	1.425	1.575	V
Input impedance					40 typical		kΩ
Positive reference voltage	REF+				2.5 typical		V
Negative reference voltage	REF-				0.5 typical		V
Reference difference, REF+ - REF-	ΔREF				2 typical		V
Accuracy, internal reference					5 typical		%
Temperature coefficient	TC				40 typical		ppm/ °C
Voltage coefficient	VC				200 typical		ppm/V
Analog inputs section							
Positive analog input	IN+		1/	All	0	AV_{DD}	V
Negative analog input	IN-				0	AV_{DD}	V
Analog input voltage difference		ΔAin = IN+ - IN-, V_{ref} = REF+ - REF-			-Vref	Vref	V

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Analog inputs section – continued.							
Input impedance			1/	All	25 typical		kΩ
PGA range					0	7	dB
PGA step size					1 typical		dB
PGA gain error						±0.25	dB
Digital inputs section							
High level digital input	V_{IH}		1/	All	2		V
Low level digital input	V_{IL}					0.8	V
Input capacitance	C_{IN}				5 typical		pF
Input current	I_{IN}					±1	µA
Digital outputs section							
High level digital output	V_{OH}	I_{OH} = 50 µA	1/	All	2.6		V
Low level digital output	V_{OL}	I_{OL} = 50 µA				0.4	V
Output current, high impedance	I_{OZ}					±10	µA
Clock timing (CS low) section							
Clock frequency	f_{CLK}		1/	01	0.1 2/	1	MHz
				02	0.1 2/	3	
				03	0.1 2/	8	
Output delay time	t_d			All		25	ns
Latency					9.5 typical		Cycles

1/ For device types 01 and 02, -40°C ≤ T_A ≤ +125°C. For device type 03, -55°C ≤ T_A ≤ +125°C. Unless otherwise specified, AV_{DD} = DV_{DD} = 3.3 V

2/ This parameter is not production tested.

Case X

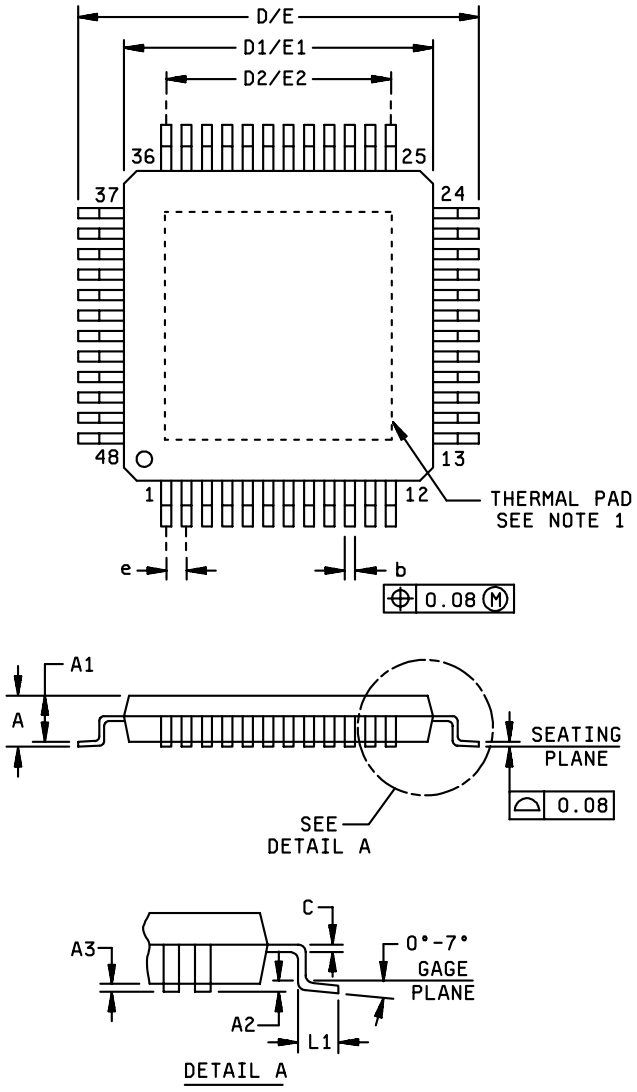

FIGURE 1. Case outlines.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03608
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Case X

Symbol	Dimensions	
	Millimeters	
	Min	Max
A		1.20
A1	0.95	1.05
A2	0.25	---
A3	0.05	0.15
b	0.17	0.27
C	0.13	---
D	8.80	9.20
D1	6.80	7.20
D2	5.50	---
E	8.80	9.20
E1	6.80	7.20
E2	5.50	---
e	0.50	---
L1	0.45	0.75

NOTES:
1. The package thermal performance may be enhanced by bonding the thermal pad to an thermal plate. This pad is electrically and thermally connected to the backside of the die and possible selected leads.
2. Body dimensions do not include mold flash or protrusion.

FIGURE 1. Case outlines – Continued.

Device types	All		Device types	All
Case outline	X		Case outline	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	-IN		25	DGND
2	AV_{DD}		26	DV_{DD}
3	VBG		27	D2
4	CML		28	D1
5	+REF		29	D0
6	-REF		30	DV_{DD}
7	AGND		31	DV_{DD}
8	AGND		32	CLK
9	DGND		33	DGND
10	OV		34	DGND
11	D13		35	$\overline{OE}$
12	D12		36	$\overline{WR}$
13	D11		37	$\overline{CS}$
14	DV_{DD}		38	NC
15	DGND		39	NC
16	D10		40	A1
17	D9		41	A0
18	D8		42	DV_{DD}
19	D7		43	AV_{DD}
20	DV_{DD}		44	AGND
21	D6		45	AGND
22	D5		46	AGND
23	D4		47	AV_{DD}
24	D3		48	+IN

NC = No connection

FIGURE 2. Terminal connections.

Terminal symbol	I/O	Description
A0; A1	I	Address input.
AGND		Analog ground.
AV_{DD}		Analog power supply.
CLK	I	Clock input.
CML		Reference midpoint. This pin requires a 0.1 μF capacitor to AGND.
$\overline{CS}$	I	Chip select input. Active low.
DGND		Digital ground.
DV_{DD}		Digital power supply.
D0 – D13	I/O	Data inputs / outputs.
NC		No connection. Do not use. Reserved.
+IN	I	Positive differential analog input.
-IN	I	Negative differential analog input.
$\overline{OE}$	I	Output enable. Active low.
OV	O	Out of range output
+REF	O	Positive reference output. This pin requires a 0.1 μF capacitor to AGND.
-REF	O	Negative reference output. This pin requires a 0.1 μF capacitor to AGND.
VBG	I	Reference input. This pin requires a 1 μF capacitor to AGND
$\overline{WR}$	I	Write signal. Active low.

FIGURE 2. Terminal connections – Continued.

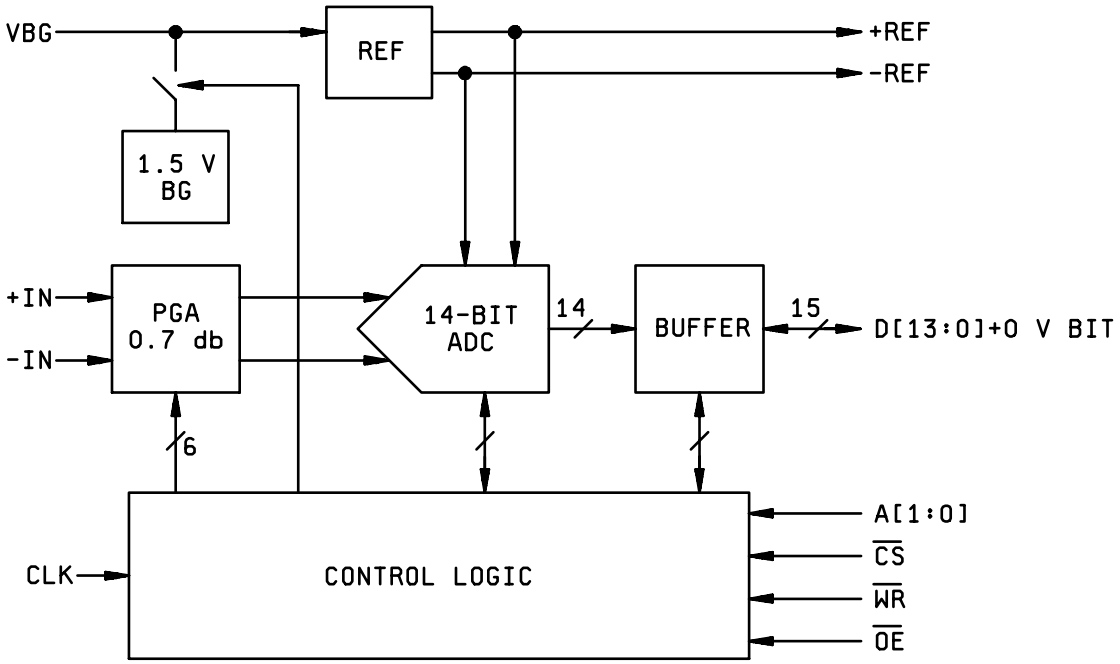
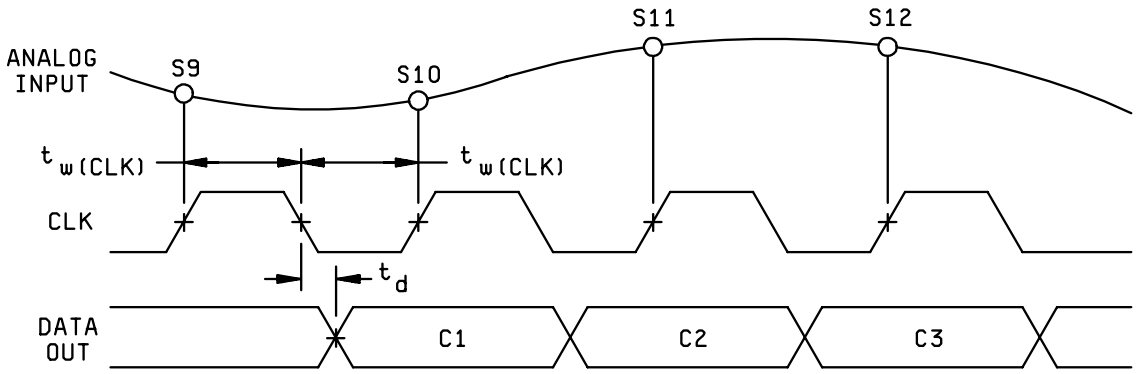


FIGURE 3. Block diagram.

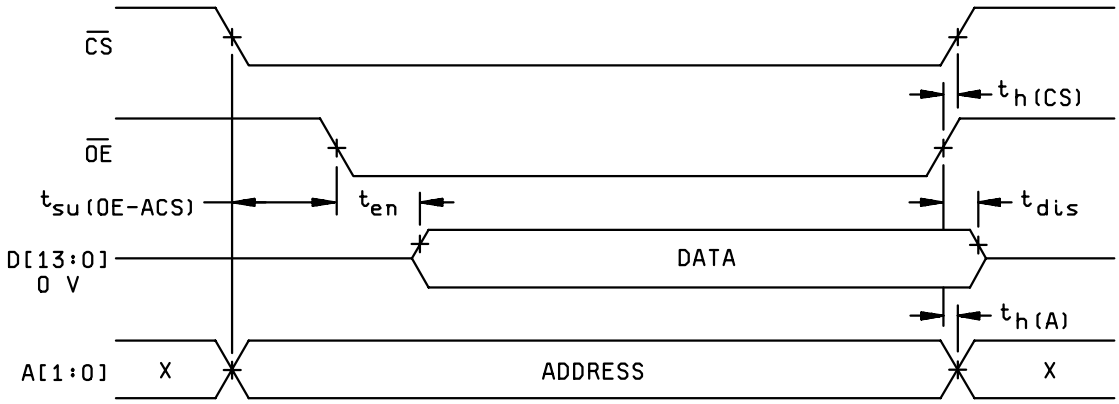
Sample timing waveform



NOTE: The device core is based on a pipeline architecture with a dormancy of 9.5 samples. The conversion results appear on the digital output of 9.5 clock cycles after the input signal was sampled. The parallel interface of the device features 3-state buffers making it possible to directly connect it to a data bus. The output buffers are enabled by driving the OE input low. Besides the sample results, it is also possible to read the values of the control register, the PGA register, and the control register. Which register is read is determined by the address inputs A1, A0. The device results are available at address 0.

FIGURE 4. Timing diagram.

Read timing waveform

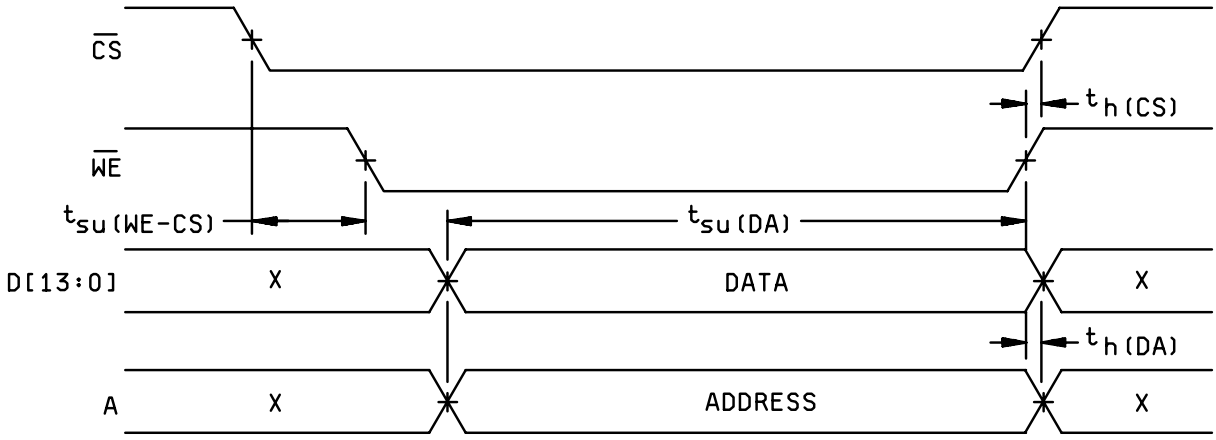


Test 1/	Symbol	Limit		Unit
		Min	Max	
Load capacitance	C_L		15	pF
Address and chip select setup time	$t_{su(OE-ACS)}$	4		ns
Output enable	t_{en}		15	ns
Output disable	t_{dis}	10 typical		ns
Address hold time	$t_{h(A)}$	1		ns
Chip select hold time	$t_{h(CS)}$	0		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

Write timing waveform



Test 1/	Symbol	Limit		Unit
		Min	Max	
Load capacitance	C_L		15	pF
Chip select setup time	$t_{su(WE-CS)}$	4		ns
Data and address setup time	$t_{su(DA)}$	29		ns
Data and address hold time	$t_{h(DA)}$	0		ns
Chip select hold time	$t_{h(CS)}$	0		ns
Wide pulse duration high	$t_{WH(WE)}$	15		ns

1/ All timing tests refer to 50 % level.

FIGURE 4. Timing diagram – Continued.

Registers

The device contains several registers. The A register is selected by the values of bits A1 and A0:

A1	A0	Register
0	0	Conversion result
0	1	PGA
1	0	Offset
1	1	Control

TABLE A and B describe how to read the conversion results and how to configure the data converter. The default values (where applicable) show the state after a power-on reset.

TABLE A. Conversion result register, Address O, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	MSB	---	---	---	---	---	---
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB

The output can be configured for two's complement or straight binary format (see D11 / control register).

The output code is given by:

2's complement:		Straight binary:	
-8192	at ΔIN = - ΔREF	0	at ΔIN = -ΔREF
0	at ΔIN = 0	8192	at ΔIN = 0
8191	ΔIN = -ΔREF – 1LSB	16383	at ΔIN = -ΔREF – 1 LSB
1 LSB	= 2ΔREF / 16384		

TABLE B. PGA gain register, Address 1, Read / Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	X
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	X	X	X	X	G2	G1	G0
Default	0	0	0	0	0	0	0

The PGA gain is determined by writing to G2-0.

Gain (dB) = 1 dB x G2-0 maximum = 7 dB. The range of G2-0 is to 0 to 7.

FIGURE 5. Principles of operation.

Registers – Continued.

TABLE C. Offset register, Address 2, Read/Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	X	X	X	X	X	X	MSB
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	---	---	---	---	---	---	LSB
Default	0	0	0	0	0	0	0

NOTE: The offset correction range is from –128 to 127 LSB. This value is added to the conversion results from the device.

TABLE D. Control Register, Address 3, Read

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES

TABLE E. Control Register, Address 3, Write

Bit	D13	D12	D11	D10	D9	D8	D7
Function	PWD	REF	FOR	TM2	TM1	TM0	OFF
Default	0	0	0	0	0	0	0
Bit	D6	D5	D4	D3	D2	D1	D0
Function	RES	RES	RES	RES	RES	RES	RES
Default	0	0	0	0	0	0	0

PWD:	Power down	0 = normal operation	1 = power down
REF:	Reference select	0 = internal reference	1 = external reference
FOR:	Output format	0 = straight binary	1 = 2's complement
TM2-0:	Test mode	000 = normal operation	
		001 = both inputs = -REF	
		010 = +IN at V_{REF} / 2, -IN at –REF	
		011 = +IN at +REF, -IN at –REF	
		100 = normal operation	
		101 = both inputs = +REF	
		110 = +IN at –REF, -IN at V_{REF} / 2	
		111 = +IN at –REF, -IN at +REF	
OF:	Offset correction	0 = enable	1 = disable
RES	Reserved	Must be set to 0	

FIGURE 5. Principles of operation – Continued.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top side marking
V62/03608-01XE	01295	THS1401QPHPEP	THS1401QE
V62/03608-02XE	01295	THS1403QPHPEP	THS1403QE
V62/03608-03XE	01295	THS1408MPHPEP	THS1408ME

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493